**REMARKS**

In the Office Action, Claims 1-7, 10-20 and 23-25 were rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,532,610 to Tsujide et al. Claims 8, 9, 21 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujide in view of United States Patent No. 6,331,782 to White et al. Applicant has amended claim 1, canceled claims 13-25, and added new claims 26-37. Applicant respectfully submits that claims 1-12, as amended, as well as new claims 26-37, are patentable and allowable over the cited art, as set forth in detail below.

**Claim 1:**

The has Examiner rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,532,610 to Tsujide et al. Claim 1 reads as follows:

> 1. A wafer-interposer assembly comprising:
>
> a semiconductor wafer including a plurality of semiconductor die, each semiconductor die having a plurality of first electrical contact pads;
>
> an interposer non-temporarily electrically and mechanically connected to the semiconductor wafer, the interposer including a plurality of second electrical contact pads respectively connected to at least some of the first electrical contact pads via conductive attachment elements such that the interposer and the semiconductor wafer are operable to be singulated into a plurality of chip assemblies; and
>
> a communication interface integrally associated with the interposer and electrically connected to at least some of the second electrical contact pads. (Emphasis added)

In the Office Action, the Examiner explained his rejection of claims 1 and 13 as follows:

> With regard to claims 1 and 13, Tsujide et al show a semiconductor wafer to be tested 1 including a plurality of die where each die has a plurality of first contact pads, an interposer which is a wafer serving as a burn-in substrate 2 which includes a plurality of second contact pads which are respectively connected to at least some of the first contact pads by attachment elements 4, 5 such that the interposer and semiconductor wafer could be singulated into chip assemblies and a communication interface 9, 23 associated with the interposer and electrically connected to at least some of the second electrical contact pads.

From a review of the disclosure of Tsujide, it can be seen that Tsujide discloses a substrate for wafer level die burn-in that is designed to form a temporary electrical connection with a wafer incorporating multiple devices under test. Figures 1 and 2 of the Tsujide reference appear as follows:

FIG. 1

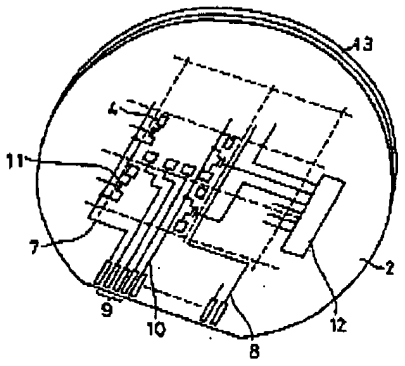
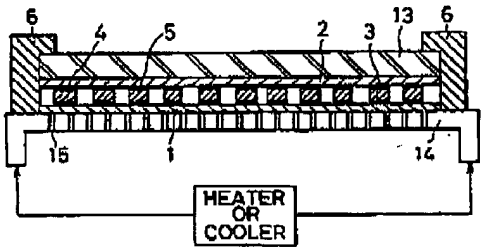



FIG. 2




Figures 1 and 2 are described by the written description of the Tsujide reference as follows:

> In FIG. 1, a wafer 2 serving as a burn-in substrate or a testing substrate is made of the same material as that of the wafer 1 to be tested, in this embodiment, silicon, and is

> supported at a bottom surface thereof by a glass substrate 13 secured thereto by, for instance, an electrostatic bonding process, to thereby enhance mechanical strength of the testing substrate. **On a front surface of the testing substrate 2 are formed pads 4 which have anisotropic conductive layers 5 provided thereon and are positioned so that the pads 4 are disposed in alignment with bonding pads 3 disposed on each of the semiconductor chips 30 formed on the wafer 1 when the testing substrate 2 is overlaid on the wafer 1.** On the testing substrate 2, from the pads 4 extend lead wires such as a line 7 to be connected to a power supply, a ground line 8, an I/O line 9 and a chip selecting line 10, each working in accordance with a function of the pad 4 from which the line extends. (Column 4, lines 38-55, emphasis added).
>
> In use of the apparatus in accordance with the invention, as illustrated in FIG. 2, the wafer 1 to be tested is placed on a stage 14 having a plurality of holes 15. **Then, the testing substrate 2 illustrated in FIG. 1 is overlaid on the wafer 1 so that the glass substrate 13 of the testing substrate 2 faces upward.** The curvature of the wafer 1 to be tested can be corrected by vacuum-chucking the wafer 1 to the substrate 2. **A fixture 6 compressively fixes the wafer 2 at a periphery thereof, so that the pads 3 disposed on the wafer 1 to be tested are in electrical connection with the pads 4 disposed on the testing substrate 2 through the anisotropic conductive layers 5 provided on the pads 4.** Then, a specific chip disposed on the wafer 1 to be tested is activated by an external signal transmitted through the testing substrate 2, to thereby obtain a desired output. (Column 5, lines 4-19, emphasis added).

Upon a review of Tsujide, Applicant respectfully submits that the Tsujide reference does not anticipate claim 1, as it fails to disclose each and every element recited in claim 1.

Specifically, Applicant respectfully submits that, contrary to the Examiner's assertion, claim 1 fails to recite an apparatus in which the interposer and semiconductor wafer "are operable to be singulated into a plurality of chip assemblies." Upon viewing the above figures of Tsujide and reading the associated written description, one of skill in the art would arrive at the

inescapable conclusion that the "substrate 2" is electrically "connected," if at all, only temporarily to the "wafer 1" solely to allow testing of the chips of "wafer 1". Further, upon a review of the teachings of Tsujide, Applicant respectfully submits that Tsujide does not teach that "substrate 2" is at any point mechanically "connected" to "wafer 1". To the extent that "substrate 2" of Tsujide could be considered to be mechanically "connected" to the "wafer 1", this relationship is also temporary.

The test fixture of Tsujide and Applicant's wafer interposer represent fundamentally different approaches to wafer level testing. The test fixture of Tsujide is designed to test multiple wafers in quick succession, making a set of temporary electrical connections between the substrate 2 and each member a set of wafers 1. In the context of the present invention as claimed, a non-temporary electrical and mechanical connection is formed between the wafer and interposer. In the present disclosure, solder balls are presented as a manner of accomplishing this non-temporary electrical and mechanical connection. This non-temporary electrical and mechanical connection is formed prior to testing of the wafer and is maintained through singulation of the wafer, at which point the interposer and wafer chip together become component parts of a chip assembly that can then be attached to a substrate. This is shown clearly in Figures 15 and 16 of Applicant's disclosure, shown below for reference.

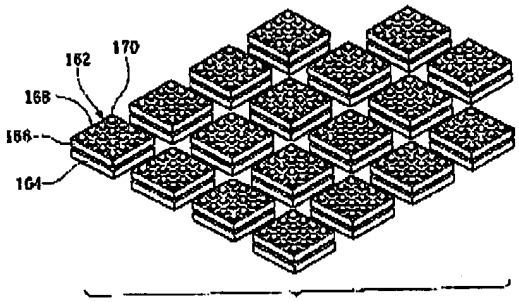



Fig.15

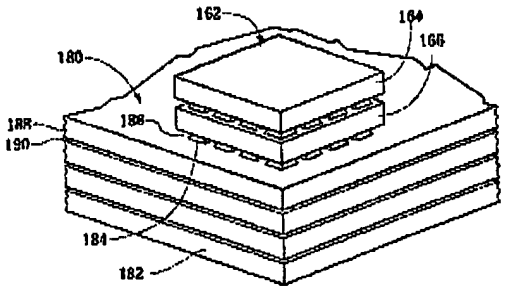



Fig.16

Applicant's disclosure describes Figures 15 and 16 as follows:

> [0060] FIGURE 15 shows an array of **chip assemblies 162**, after singulation of the wafer-interposer assembly 140 (FIGURE 14). **Each chip assembly 162 comprises a chip 164, an interposer 166 and a plurality of conductive attachment elements 170 deposited on the conductive pads 168 on the exposed surface of the interposer 166.** The chip assemblies 162 will be separated into conforming and non-conforming groups or sorted by performance level according to the results of the wafer level testing described in accordance with FIGURE 3. The wafer-interposer assembly 140 (FIGURE 14) can be singulated into groups of chip assemblies 162 instead of individual die.
>
> [0061] FIGURE 16 shows an assembly 180 comprising a chip assembly 162 mounted on a substrate 182 having a plurality of conductive layers 190 and dielectric layers 188. The chip assembly 162 is electrically and mechanically attached to pads 184 on the surface of the substrate 182 through conductive attachment elements 186. The chip assembly 162 communicates with other electronic devices (not shown) through the conductive layers 190 of the substrate 182. Assembled as shown, the interposer 166 provide electrical connection between chip 164 the substrate 182.

In contrast to the above figures and written description, which explicitly depict and describe non-temporary electrical and mechanical connections between the chips 164 and sections of

interposer 166, there is nothing permanent or non-temporary about the contact between substrate 2 and wafer 1 of Tsujide. Each substrate 2 of Tsujide is designed to be re-used with each member of a set of individual wafers 1. They are not attached to one another in a non-temporary manner, either electrically or mechanically. If an attempt were made to singulate the wafer 1 and substrate 2 of Tsujide into a plurality of chip assemblies, the result would be a plurality of wafer chips and a plurality of substrate chips, but the individual wafer chips and substrate chips would not be connected to one another and would therefore not be "chip assemblies" as that term is used within the context of the present application. Accordingly, the substrate 2 and the wafer 1 of Tsujide are not "operable to be singulated into a plurality of chip assemblies" as that language is used within the context of the present disclosure. For the same reasons as elaborated above, Tsujide does not disclose an interposer "non-temporarily electrically and mechanically connected to the semiconductor wafer", as recited in amended claim 1. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b) rejection and allowance of claim 1.

**Claims 2-12**

Claims 2-12 depend from claim 1 and add further limitations. Accordingly, each of claims 2-12 is allowable as being dependent on

an allowable independent claim. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b) and §103 rejections of claims 2-12.

Claim 26

As noted above, the Tsujide reference fails to teach or suggest that the substrate 2 and the wafer 1 of Tsujide are "operable to be singulated into a plurality of chip assemblies" as recited in newly-added independent claim 26. Similarly, Tsujide does not disclose an interposer having a pattern of second electrical contact pads "non-temporarily electrically and mechanically connected to at least some of the first electrical contact pads", as recited in new claim 26. Further, claim 26 recites additional limitations not present in claim 1 which further distinguish this claim from Tsujide. Accordingly, Applicant respectfully requests allowance of newly-added independent claim 26.

Claims 27-37

Claims 27-37 depend from claim 26 and add further limitations. Accordingly, each of claims 27-37 is allowable as being dependent on an allowable independent claim. Accordingly, Applicant respectfully requests allowance of claims 27-37.

## Conclusion

In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections to claims and allow claims 1-12 and 26-37 presented for consideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested. The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 26th day of January, 2005.

Respectfully submitted:

Lawrence R. Youst
Reg. No. 38,795
Danamraj & Youst, P.C.
Premier Place, Suite 1450
5910 North Central Expressway
Dallas, Texas 75206
Tel 214.363.4266
Fax 214.363.8177